REMARKS

Claims 1-23 will be pending in the current Application. Claims 1, 2, 5, 6, 8, 9, and 11-14 have been amended; and claim 23 has been added. Note that claims 1, 2, 5, and 6 have been amended to correct a typographical error by replacing register elements with data elements in order to maintain better consistency within the claims, and not for prior art reasons. Applicant submits that the amendments do not add new matter to the current Application. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Provisional Nonstatutory Obviousness-Type Double Patenting Rejection

Applicant respectfully submits that claims 1-22 are patentably distinct over Application No. 10/657,797. However, in order to further prosecution, Applicant is submitting concurrently herewith a terminal disclaimer to obviate the obviousness double-patenting rejection over Application No. 10/657,797. Applicant also respectfully submits that claims 1-22 are patentably distinct over Application No. 10.657,510. However, in order to further prosecution, Applicant is submitting concurrently herewith a terminal disclaimer to obviate the obviousness double-patenting rejection over Application No. 10/657,510. Therefore, Applicant respectfully requests that the Examiner withdraw the provisional rejection of obviousness-type double patenting.

Rejection of claims 1-16 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1-16 are patentable over US Patent No. 5,870,596 (hereinafter referred to as Yoshida) because Yoshida does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claim 1, claim 1 includes at least one or more instruction specifying a number of data elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory. (Note that "register elements"

has been amended to read "data elements" so as to provide greater consistency within claim 1). That is, the number of data elements specified corresponds to the number of data elements transferred between *each register* of the at least two registers and memory, where, as claimed in claim 1, "*each* general purpose register *holds multiple data elements*." Therefore, the number of data elements refers to a number of data elements ***within*** a particular general purpose register. Yoshida at least does not teach or suggest the number of data elements as claimed. The Examiner cites that col. 24, lines 14-21, which describes the loading of 4 bytes according to internal code LDM1 to R1, and col. 24, lines 45-50 which describes the loading of 4 bytes into registers R4 according to internal code LDM2. However, note that the number of elements loaded into each registers (R1 and R2) is always 4. That is, there is no field or specifier provided in the LDM instruction to specify this number. For example, as described in col. 10, lines 10-11 and lines 22-23 with respect to the LDM and STM instructions, the data transferred to and from each of the registers is respectively 4 bytes. Therefore, any number of *registers* (and ***not*** data elements) can be specified in which to load from or store to, but the data transferred to/from each register is always 4 bytes. Therefore, there is no teaching or suggestion of specifying a number of data elements to be transferred to or from each register, as claimed. Furthermore, one would not be motivated to do so, since the data transferred in Yoshida is fixed to 4 bytes. Therefore, for at least these reasons, Applicant submits claim 1 is allowable over Yoshida.

The Examiner, in addressing this argument in the current Office Action (argument "c" in paragraph 13), states that "since the register had a limited data size, the number of register elements had to be specified in order to keep data transfer of always 4 bytes." And the Examiner then proceeds to provide the example "if one register had 2 bytes in size, two registers would be 4 bytes total." However, Yoshida does not teach or suggest this as a possibility. That is, the size of the registers in Yoshida is 4 bytes, and that is why 4 bytes is always transferred. That is, nothing in Yoshida teaches or even suggests the possibility of transferring 4 bytes of data to/from *two* or more registers, it only discusses transferring 4 bytes of data to/from *one* register. Furthermore, the Examiner proceeds to state, after providing this example, that "therefore, in order to keep transfer of always 4 byte, the *number of register* had to be specified" (emphasis added). Firstly, as already discussed above, there is no need to specify the number of register *to keep the transfer of always 4 bytes* because in Yoshida, the transfer is always 4 bytes per register,

regardless of the number of registers specified. Furthermore, claim 1 claims specifying "the number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory" where, as also claimed in claim 1, "each general purpose register holds multiple data elements." That is, secondly, the Examiner's statement of "the number of registers had to be specified" is irrelevant because the at least one instruction of claim 1 is not simply identifying a number of *registers* but a number of data elements ***in each*** register, where this number may specify a number indicating all of the data elements within each register or less than all data elements within each register. Note that since Yoshida always transfers all 4 byte to/from a single register, there is never any number used to identify a number of data elements within the register, and thus, less than all 4 bytes (i.e. less than all data elements) of a register can never be transferred in Yoshida. Therefore, for at least these additional reasons, Applicant submits that claim 1 is allowable over Yoshida.

With respect to claim 5, Applicants have also amended claim 5 such that "register elements" now reads "data elements" so as to provide greater consistency within claim 5. Claim 5 claims "storing *multiple data elements* in *each* of a plurality of general purpose registers" and executing at least one of the one or more instructions which "specifies a number of data elements to be transferred between *each* of the at least two of the plurality of general purpose registers and the memory." Therefore, the same arguments and rebuttals provided above with respect to claim 1 also apply to claim 5 and therefore, Applicant submits that claim 5 is also allowable over Yoshida for at least those reasons.

With respect to claim 8, Applicant has amended claim 8 to clarify that the "at least one or more instructions specifies which subset of the multiple data elements in each of the at least two of the plurality of general purpose registers are to be transferred." That is, claim 8 claims that the at least one or more instructions can specify a subset of data elements within *each* of the at least two registers. As discussed above in reference to claim 1, the number of data elements within each register that is transferred is always 4 bytes, where each register holds only 4 bytes. That is, there is no teaching or suggestion in Yoshida to specify a number within an instruction that is capable of transferring a subset of multiple data elements that is held in a register. Therefore, for at least these reasons, Applicant submits that claim 8 is allowable over Yoshida.

With respect to claim 13, Applicant has amended claim 13 in a way similar to the amendments to claim 8. Therefore, the arguments provided above with respect to claim 8

also apply to claim 13. Therefore, for at least those reasons, Applicant submits that claim 13 is allowable over Yoshida.

With respect to claim 15, Applicant submits that Yoshida does not teach or suggest each and every element of claim 15. For example, claim 15 includes "a plurality of general purpose registers wherein each general purpose register holds multiple data elements" and processor circuitry for executing one or more instructions which "specifies both a number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory and further specifies a total number of data elements to be transferred." At least this is not taught or suggested by Yoshida. That is, as discussed above in reference to claims 1, 5, 8, and 13, Yoshida does not teach or suggest specifying a number of data elements ***within each*** of at least two general purpose registers to be transferred. Furthermore, Yoshida does not teach or suggest specifying both this number of data elements within each register of at least two registers to be transferred in addition to specifying a total number of *data elements* to be transferred. That is, claim 15 also claims specifying a total number of data elements (rather than a number of registers) to be transferred, which is also not taught or suggested by Yoshida. Therefore, for at least these reasons, Applicant submits that claim 15 is allowable over Yoshida.

Claims 2-4, 6, 7, 9-12, 14, and 16 have not been independently addressed since they depend directly or indirectly from allowable claims 1, 5, 8, 13, or 15, and are therefore patentable over Yoshida for at least those reasons provided above with respect to these claims. Furthermore, added claim 23 also depends from allowable claim 1, and is therefore allowable for at least those reasons provided above with respect to claim 1.

Rejection of claims 1-22 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1-22 are patentable over US Patent No. 6,170,001 (hereinafter referred to as Hinds) because Hinds does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claims 1, 5, and 15, each of claims 1, 5, and 15 includes at least one or more instruction specifying a number of data elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory, where *each* general purpose register *holds multiple data elements*. (Note that "register

elements" has been amended to read "data elements" in claims 1 and 5 so as to provide greater consistency within these claims). That is, the number of data elements specified corresponds to the number of data elements transferred between *each register* of the at least two registers and memory. Therefore, the number of data elements refers to a number of data elements ***within*** a particular general purpose register. Hinds at least does not teach or suggest the number of register elements as claimed. The Examiner cites that col. 2, lines 60-67, which describes the number of odd data words, and col. 10, lines 54-64 which describes the use of a data type bit specifying the use of single or double precision. However, neither the number of odd data words nor the data type bit which simply indicates the use of single or double precision teach or suggest a number of data elements transferred to/from *each* register, as claimed. The Examiner further points to col. 20, lines 11-48 for the detail of operand data elements in a bank of registers, however, no details are provided of an instruction. This section describes operation of the VFPv1 (a floating point system architecture) which provides access to the registers in either scalar or vector mode. However, no instruction specifying the number of registers elements as claimed is discussed. Therefore, for at least these reasons, Applicant submits claims 1, 5, and 15 are allowable over Hinds.

The Examiner, in addressing this argument in the current Office Action (argument "g" in paragraph 14), states that "no number of register elements refers to a number of register elements within a particular general purpose register can be found in the claims." Applicant respectfully disagrees. Firstly, as discussed above, Applicant has amended each of claims 1 and 5 to clarify that the at least one or more instructions specifies a number of data elements to be transferred rather than a number of register elements. Therefore, since ***each*** general purpose register is claimed as holding *multiple data elements*, the number of data elements to be transferred between ***each*** of at least two general purpose registers and the memory clearly indicates that the number of data elements refers to a number of data elements within a particular general purpose register. Therefore, for these additional reasons, Applicant submits that claims 1, 5, and 15 are allowable over Hinds.

With respect to claim 8, Applicant has amended claim 8 to clarify that the "at least one or more instructions specifies which subset of the multiple data elements in each of the at least two of the plurality of general purpose registers are to be transferred." This is also not taught or suggested by Hinds. That is, claim 8 claims that the at least one or

more instructions can specify a subset of data elements within *each* of the at least two registers. Neither the odd or even number of data words of Hinds nor the VFPv1 discussed in col. 20 of Hinds specify a subset of data elements within each of at least two registers that are to be transferred. That is, there is no teaching or suggestion in Hinds to specify a number within an instruction that is capable of transferring a subset of multiple data elements that is held in a register. Therefore, for at least these reasons, Applicant submits that claim 8 is allowable over Hinds.

With respect to claim 13, Applicant has amended claim 13 in a way similar to the amendments to claim 8. Therefore, the arguments provided above with respect to claim 8 also apply to claim 13. Therefore, for at least those reasons, Applicant submits that claim 13 is allowable over Hinds.

Claims 2-4, 6, 7, 9-12, 14, and 16-22 have not been independently addressed since they depend directly or indirectly from allowable claims 1, 5, 8, 13, or 15, and are therefore patentable over Hinds for at least those reasons provided above with respect to these claims. Furthermore, added claim 23 also depends from allowable claim 1, and is therefore allowable for at least those reasons provided above with respect to claim 1.

Rejection of claims 1, 5, 8, 10, 13, and 15 under 35 U.S.C. 102(b)

Applicant respectfully submits that claims 1, 5, 8, 10, 13, and 15 are patentable over US Patent No. 4,760,545 (hereinafter referred to as Inagami) because Inagami does not teach or suggest each an every element, as required in a finding of anticipation.

With respect to claims 1, 5, and 15, each of claims 1, 5, and 15 includes at least one or more instruction specifying a number of data elements to be transferred between ***each*** of the at least two of the plurality of general purpose registers and the memory, where *each* general purpose register *holds multiple data elements*. (Note that "register elements" has been amended to read "data elements" in claims 1 and 5 so as to provide greater consistency within these claims). That is, the number of data elements specified corresponds to the number of data elements transferred between ***each register*** of the at least ***two*** registers and memory. Therefore, the number of data elements refers to a number of data elements ***within each*** of at least two general purpose registers. Inagami at least does not teach or suggest the number of data elements as claimed. The Examiner refers to fig. 4b, stating that "L" is the number of vector elements to be transferred. The

Examiner also refers to col. 6, lines 52-68 as providing the number specified by instruction. However, although L specifies a number of vector elements, the value L specifies a number of vector elements to be transferred to or from a single vector register, denoted by R1 in FIG. 4b, and thus the value L does not specify a number of data elements transferred to/from ***each*** *register of at least* ***two*** *registers* as claimed. For example, FIG. 8 of Inagami provides an example of a load instruction (instruction 1) having the format of the instruction of FIG. 4b, where the L value is 102. As described in col. 13, lines 45-50, this instruction 1 instructs that 102 elements (where L=102) of the array A should be read out from main memory and successively stored from the element number 0 of the VR0 register. That is, the 102 elements (including A(0) to A(101)) are all loaded successively into VR0. There is no teaching or suggestion in Inagami to load L elements from memory into each of at least two registers. For example, with respect to instruction 1 of FIG. 8, there is no teaching or suggestion of loading "102" elements into each of at least two registers such as VR0 and another VR register. The instruction format, as illustrated in FIG. 4b, does not even allow for this possibility. Therefore, for at least these reasons, Applicant submits claims 1, 5, and 15 are allowable over Inagami.

New claim 23 depends from allowable claim 1, and is therefore also allowable over Inagami for at least those reasons provided with respect to claim 1.

With respect to claim 8, Applicant has amended claim 8 to clarify that the "at least one or more instructions specifies which subset of the multiple data elements in each of the at least two of the plurality of general purpose registers are to be transferred." This is also not taught or suggested by Inagami. That is, claim 8 claims that the at least one or more instructions can specify a *subset* of data elements within *each* of the at least *two* registers. As described above in reference to claims 1, 5, and 15, the variable L of the instruction does not teach or suggest specifying a subset of data elements within each of at least two registers, as claimed in claim 8. Therefore, for at least these reasons, Applicant submits that claim 8 is allowable over Inagami.

Claim 10 has not been independently addressed because it depends indirectly from allowable claim 8 and is therefore also allowable for at least those reasons provided with respect to claim 8.

With respect to claim 13, Applicant has amended claim 13 in a way similar to the amendments to claim 8. Therefore, the arguments provided above with respect to claim 8

also apply to claim 13. Therefore, for at least those reasons, Applicant submits that claim 13 is allowable over Inagami.

Conclusion

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants.

Applicants respectfully solicit allowance of the pending claims. Should there be any issues regarding this communication or the current Application, please feel free to contact me.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: 

Joanna G. Chiu
Attorney of Record
Reg. No.: 343,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125